

E1
Cont.

a differential circuit having a first transistor and a second transistor to generate a differential output signal having a logic level, a first gate of the first transistor receiving the data strobe signal, a second gate of the second transistor receiving a reference signal, and sources of the first and second transistor being connected in common and having the same potential,

a current mirror circuit supplying a current to the differential circuit,
a constant current source coupled to the sources of the first and second transistors, and
a current adjustment transistor coupled to the sources of the first and second transistors, a third gate of the current adjustment transistor receiving the differential output signal of the differential circuit, wherein the current adjustment transistor turns ON and OFF in response to the logic level of the differential output signal such that a falling delay time and a rising delay time of the logic level of the differential output signal are substantially the same.

REMARKS

The Office Action dated October 7, 2003 has been received and carefully noted. The Applicant notes with appreciation, the Examiner's indication that claims 1-2, 4-20 are allowable. The above amendments and following remarks are submitted as a full and complete response thereto. By this Response, claim 21 is amended. Support for the amendments can be found at page 10, lines 30-32 of the specification. No new matter is added. Accordingly, claims 1, 2 and 4-21 are respectfully submitted for consideration.